REMARKS

I. Introduction

Applicants have amended claims 11, 14 and 15 to further clarify the subject matter of the present invention. Support for the amendment to claims 11, 14 and 15 may be found, for example, on page 24, lines 15-26. No new matter has been added.

Applicants note with appreciation the indication of allowable subject matter being recited by claims 13 and 16.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of Claims 11, 12, 14 And 15 Under 35 U.S.C. § 103

Claims 11, 12, 14 and 15 were rejected under 35 U.S.C. § 103(a), as being unpatentable over Jarwala et al. (USP No. 5,673,276) in view of Komoike (USP No. 6,094,736). Applicants respectfully traverse these rejections for at least the following reasons.

Claim 11, as amended, recites, in part, a semiconductor device comprising: a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material, having a wiring layer; a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto; a boundary scan test circuit provided in each of said chip IPs; an internal combinational circuit provided in each of said chip IPs; and an internal scan chain for an internal scan test provided in each of said chip IPs, wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an internal scan test simultaneously with each

other for testing said combinational circuit, using test data for an internal scan test which is input from outside.

With respect to claim 11, the Examiner alleges that Jarwala discloses a boundary scan test circuit provided in each of a plurality of chip IPs and an internal scan chain for an internal scan test. Furthermore, he suggests that it is possible to operate them simultaneously during an internal scan test.

However, Jarwala teaches a structure which enables a hierarchical boundary scan test with respect to the entire MCM when an IP chip with a boundary scan test circuit is mounted on an MCM with a boundary scan test circuit. There is no teaching or suggestion in Jarwala that discusses an internal scan test, a technique for testing the inside of each chip on an individual basis. As is shown in column 8, lines 26-40 and column 9, lines 31-43, the reference numeral 52' in figures 9 and 12 of Jarwala, the boundary scan register mounted on a chip 14 ("internal" register element refers to a boundary scan register on the internal chip 14 in a MCM) corresponds to a reference numeral 69 in figures 10 and 11 of the present invention, not the "internal scan chain for internal scan test" corresponding to a reference numeral 71 in figures 10 and 11 of the present invention. As such, it is clear that the alleged internal scan chain referred to in the Office Action in col. 5, lines 62-65 Jarwala is a boundary scan chain, not an internal scan chain. Furthermore, the passage referred to which allegedly describes that the internal scan chain is for an internal scan test (col. 4, lines 36-37, Jarwala) actually describes a boundary scan test. Thus, Jarwala fails to disclose an internal scan chain for an internal scan test provided in each of said chip IPs, wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so as to be capable of performing a boundary scan test and an

internal scan test simultaneously with each other for testing said combinational circuit. Komoika does not cure this deficiency of Jarwala, and is not relied upon as doing so.

Amended claim 14 recites a semiconductor device comprising...a scan-in terminal for inputting test data for an internal scan test directly from said at least two pieces of wiring to said boundary scan test circuit of at least one of said chip IPs, and a scan-out terminal for outputting a test result of an internal scan test directly to outside from said boundary scan test circuit of at least one of said chip IPs.

It is alleged that Jarwala anticipates each of the limitations of claim 14 of the present invention. However, claim 14, as currently amended, is characterized in that a scan-in terminal and a scan-out terminal for an internal scan test are provided in addition to the input terminal (TDI) and the output terminal (TDO) for a boundary scan test. Nowhere in Jarwala is there any mention of a scan-in terminal or scan-out terminal for an internal scan test. Furthermore, Komoike fails to correct this deficiency. Accordingly, neither Jarwala nor Komoike disclose the above-recited limitations of claim 14.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA1974). As Jarwala and Komoike both fail to teach or suggest a semiconductor device comprising: a semiconductor wiring substrate, said semiconductor wiring substrate being composed of a semiconductor material, having a wiring layer; a plurality of chip IPs mounted on said semiconductor wiring substrate by being bonded thereto; a boundary scan test circuit provided in each of said chip IPs; an internal combinational circuit provided in each of said chip IPs; and an internal scan chain for an internal scan test provided in each of said chip IPs, wherein the boundary scan test circuit and the internal scan chain for an internal scan test are formed so

as to be capable of performing a boundary scan test and an internal scan test simultaneously with each other for testing said combinational circuit, using test data for an internal scan test which is input from outside OR, a semiconductor device comprising a scan-in terminal for inputting test data for an internal scan test directly from said at least two pieces of wiring to said boundary scan test circuit of at least one of said chip IPs, and a scan-out terminal for outputting a test result of an internal scan test directly to outside from said boundary scan test circuit of at least one of said chip IPs, it is submitted that Jarwala and Komoike do not render claims 11 and 14 obvious. Accordingly, it is respectfully requested that the § 103 rejection of claims 11, 14 and any pending claims dependent thereon be withdrawn.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 11 and 14 are patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Michael E. Fogarty
Registration No. 36,139

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 MEF/NDM:kap
Facsimile: 202.756.8087
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